3. (Original) The memory array as recited in claim 1, wherein depending on electrical signals generated outside the memory array, the circuit combines data read out from the read sense amplifier and data received from outside the memory array to make it available to the write data driver.

4. (Original) The memory array as recited in claim 1, wherein the write wordlines are coupled to the write activation terminals of the memory cells, the write wordlines being positioned orthogonally to the read and write bitlines, and wherein the plurality of read wordlines are connected to the read activation terminals of the memory cells and positioned orthogonally to the read and write bitlines.

5. (Original) The memory array as recited in claim 3, wherein the read and write wordlines are asserted by a wordline decoder and by corresponding write data drivers, and wherein one read wordline and one write wordline are asserted simultaneously for different cells of the memory array.

6. (Original) The memory array as recited in claim 3, wherein the circuit associated with each read sense amplifier and write data driver holds data sensed by the read sensing amplifier, providing a means for allowing data read-out of the array during one cycle to be modified and written-back to the memory array concurrently with the read-out operation of the next memory cycle.

7. (Original) The memory array as recited in claim 6, wherein the write cycle consists of read-out and write-back phases.